We claim:

1. A method for transmitting a control signal on a bus, said control signal having two signal states, said method comprising the steps of:

transferring a first signal state for said control signal by adjusting a voltage level from a previous time interval; and

transferring a second signal state by maintaining said voltage level from the previous time interval.

2. The method of claim 1, further comprising the step of maintaining said voltage level from the previous time interval using a memory element.

3. The method of claim 1, further comprising the step of ensuring that only a single node connected to said bus can assert said control signal in a given time interval.

4. The method of claim 1, wherein said bus is on a system-on-chip (SoC).

5. The method of claim 1, wherein said bus is on a printed circuit board (PCB).

6. The method of claim 1, wherein said adjusting step further comprises the step of transitioning from a first voltage level to a second voltage level.

7. The method of claim 1, wherein said adjusting step further comprises the step of applying a high logic level to an exclusive-OR gate with said voltage level from the previous time interval to determine the signal level to be asserted in the current time interval.

8. A method for receiving a control signal on a bus, said control signal having two signal states, said method comprising the steps of:

detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted; and

detecting a second signal state if said voltage level from the previous time interval is maintained.

9. The method of claim 8, further comprising the step of maintaining said control signal value at said voltage level from said previous time interval when no node drives said bus.

10. The method of claim 9, further comprising the step of compensating for leakage and cross-coupling effects.

11. The method of claim 8, further comprising the step of maintaining said voltage level from the previous time interval using a memory element.

12. The method of claim 8, wherein said bus is on a system-on-chip (SoC).

13. The method of claim 8, wherein said bus is on a printed circuit board (PCB).

14. The method of claim 8, wherein said adjusted voltage level is a transitioning from a first voltage level to a second voltage level.

15. The method of claim 8, wherein said first detecting step further comprises the step of applying said received control signal state to an exclusive-OR gate with said voltage level from the previous time interval to determine the signal level to be asserted in the current time interval.

16. A device for communicating a control signal on a bus, said control signal having two signal states, said device comprising:

a memory element for maintaining a voltage level from a previous time interval;

a comparison circuit for detecting a change in said voltage level from the previous time interval indicating an assertion of said control signal by another device; and

an adjustment circuit for changing said voltage level from the previous time interval indicating an assertion of said control signal by another device.

17. The device of claim 16, wherein said memory element is a latch.

18. The device of claim 16, further comprising a circuit that ensures that only a single device connected to said bus can assert said control signal in a given time interval.

19. The device of claim 16, wherein said bus is on a system-on-chip (SoC).

20. The device of claim 16, wherein said bus is on a printed circuit board (PCB).

21. The device of claim 16, wherein said change in said voltage level from the previous time interval is a change from a first voltage level to a second voltage level.

22. The device of claim 16, wherein said adjustment circuit is an exclusive-OR gate.

23. The device of claim 16, wherein said comparison circuit is an exclusive-OR gate.